Series Pass Transistor Design Considerations

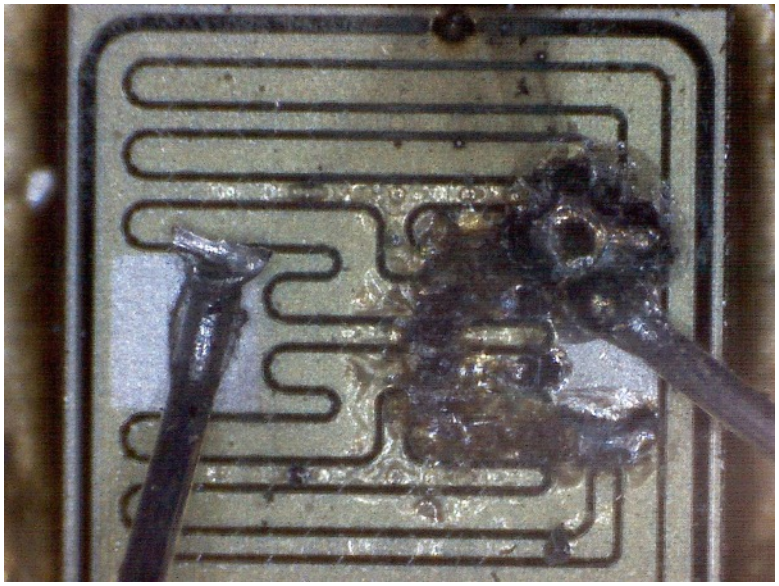
1.0 Introduction

After successfully completing many PS-15D-( ) power supplies, a new problem presented itself during a refurbish of an Astron RS-20M. Astron uses 2 each 2N3771 series pass transistors, which in this power supply, had both failed with with a Base to Collector short.

I did not give much thought to these failures because this power supply had multiple problems and I was going to strip the unit down to bare chassis and refurbish with my PS-15D-102 regulator board. Once refurbished, the new power supply worked perfect as expected. However, a few minutes into load testing with a 15.0 ADC Electronic Load, both pass transistors failed again; shorted B-C.

Presented in this paper is an explanation of the failures and what design changes need to be made to prevent this transistor failure mode.

Shown below is one of the damaged transistors from the Astron RS-20A showing melted silicon and area or B-C short.



Series Pass Transistor Design Considerations

2.0 Pass Element Topology

Figure 2.1 is a simplified schematic of the PS-15D-( ) Pass Transistors. Shown here is the representation of the 2 transistor Astron RS-20M refurbish configuration. These Pass Transistors are arranged in the common Emitter configuration, whereas the Astron uses a common Collector configuration (Emitter Follower).

However, the following analysis indicates the failure mode is not significantly affected by the circuit configuration, but rather by the thermal design.

Figure 2.1 shows the rectified and filtered DC voltage is applied across the series combination of R_L, each transistor's C-E and R_E. Ideally the least possible voltage should be presented across the transistors in order to reduce their power dissipation. A trade-off is required to satisfy low line voltage and minimum V_{CE} requirement vs power dissipation.

Astron uses an emitter follower pass element, which inherently requires a higher V_{CE} than the PS-15D-20A design. As a matter of fact the rectified DC Voltage is higher than necessary for most line conditions, and therefore a buck transformer is normally inserted into the primary winding when refurbishing Astrons.

In the case of the Astron RS-20M, there is not enough room within the chassis for a buck transformer, so this refurbish uses the too high rectified voltage.

3.0 Astron Pass Transistor Failures

RS-20M Astron is a 16 ADC continuous output power supply, 20A reduced duty cycle.

Figure 2.1 shows a simplified schematic of the pass transistors with $R_E = 0.10\Omega$.

$$V_{RECT} = 20.85 \text{ VDC},$$
$$I_O = 15 \text{ ADC},$$

Each Pass Transistor power dissipation is given by;

$$P_D = V_{CE} \times I_C + V_{BE} \times (I_C \div \beta).$$

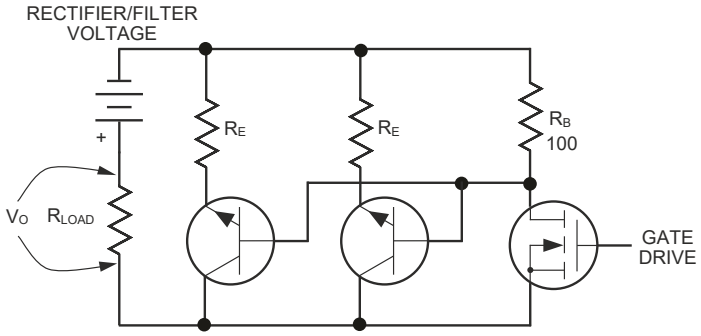


Figure 2.1. Pass Transistors simplified schematic.

Because the term $V_{BE} \times (I_C \div \beta)$ represents the Base power dissipation, and even with very low β represents less than a 0.5W contribution, it will be ignored.

$$\text{So, } P_D = V_{CE} \times I_C.$$

Refer to Figure 2.1 to see that;

$$V_{CE} = V_{RECT} - V_O - V_E, \text{ and}$$

$$V_{CE} = 20.85 - 13.85 - (7.5A \times 0.10\Omega), \text{ or}$$

$$V_{CE} = 6.25V$$

It is reasonable to assume the two transistors divide the load current equally, therefore;

$$PD = V_{CE} \times I_C, \text{ and}$$

$$PD = 6.25V \times 7.5A$$

$$PD = 46.88W,$$

and of course the heat sink dissipation is;

93.76W.

The junction temperature is given by[1];

$$T_J = P_D \times (\Theta_{JC} + \Theta_{CS}) + T_S \text{ and,}$$

$T_J = 46.88W \times (1.17^oC/W + 0.33^oC/W) + T_S$, and

$T_J = 70.32\,^oC + T_S$.

These calculations show the transistor junction temperature is 70.32 °C greater than the heat sink temperature. To determine the heat sink temperature, three variables must be known; 1, the heat sink θ_{SA}, 2. the maximum ambient temperature allowable and 3. the total power dissipation of the heat sink.

Previously calculated power dissipation = 93.76W, however, that value is for the power transistor dissipation only. The Astron RS-20M also has the rectifier diodes (a packaged bridge) mounted to the common heat sink. Using the BWC Electronics "Rectifier Design and Analysis" the rectifier power dissipation for a 15 ADC output load and 120 VAC input is 23.55W.

Therefore the total heat sink dissipation is;

$P_{D(total)} = 93.76 + 23.55W$

$= 117.31W.$

Astron uses a custom heat sink, so finding a value for θ_{SA} is not possible. Two similar heat sinks in terms of volume and area are the Thermalloy 16544 and the HeatsinksUSA 7-280 both of which have $\theta_{SA} = 1.3^oC/W$ for a 3 inch length. Using Figure 3 graph from reference 1, then θ_{SA} for 4" = 0.87 x $1.3^oC/W$ or $1.13^oC/W$ for the length heat sink used in the Astron RS-20M.

Thus the heat sink temperature, for a given maximum ambient operating temperature, is given by:

$T_S = P_D \times \Theta_{SA} + T_A$ and,

$T_S = 117.31W \times 1.13^oC/W + 40^oC$, or

$T_S = 172.56^oC$, and

$T_J = 70.32\,^oC + 172.56^oC$, or

$T_J = 242.88\,^oC$.

An ambient temperature of 40°C (which is only 104°F) and is common around heat generating equipment, even in a 25°C room. It is easy to see that operating at elevated temperatures directly increases the junction temperature.

These calculations show the junction temperature is **121%** of the **MAXIMUM** allowed operating temperature. My Military design and Collins experience required designs limit junction temperature to 60%, or less, of the maximum operating value.

The Astron RS-20A Pass Transistor failure cause is easy to see from the above calculations. Even though the failures occurred while the power supply was operating inside the transistor's SOA, new studies (covered in Section 5) explain the failure mechanism. The designer could have avoided this less well understood failure mode by simply adhering to proper de-rating guidelines.

4.0 PS-15D-20A Pass Transistor Failures

Now, a similar analysis will show why the PS-15D-20A, which is a PS15D-102 regulator fitted into the Astron RS-20A chassis, using the two pass transistors and heat sink, failed with the same Base to Collector short.

Conditions are the same as with the Astron until the transistor case to sink temperature is calculated. For the PS-15D-20A design, the pass transistors are mounted (with thermal compound) directly to the heat sink, there is no need for mica insulators, therefore the case temperature is given by;

The junction temperature is given by[1];

$T_J = P_D \times (\Theta_{JC} + \Theta_{CS}) + T_S$ and,

$T_J = 46.88W \times (1.17^oC/W + 0.17^oC/W) + T_S$, and

$T_J = 62.82\,^oC + T_S$.

However, a 7.5°C improvement (even though worthwhile) only lowers the junction temperature to 235.38°C; still 117% of maximum allowed operating temperature.

1. θ_{CS} is based on Thermalloy Publication 90-HS-11, pg. 13, for 0.002" Mica with thermal compound mounting of a TO-3 (TO-204AA) case transistor. 6-32 mounting screw torque = 6.0 in-lbs, each.
2. Heat sink performance for Thermalloy 16544 6.496 x 3" x 1.561" fins $\theta_{SA} = 1.3^oC/3$" length. And HeatsinkUSA 7-280 for 7.20 x 3" x 1.30" fins $\theta_{SA} = 1.3^oC/3$" length. Verification that similar volume and surface heat sinks have very similar θ_{SA}.

It is now easy to see why both power supplies succumbed to the same failure mode.

5.0 Failure Mode Within the SOA

Recent research sheds light on how power transistors, operating within the SOA still fail. I did not run into this phenomenon many years ago, during my active design days. Turns out the reason may well be, that the designs of that time period included sufficient thermal design to ensure the Junction Temperature never exceeded a fraction of the maximum allowed.

As presented in sections 3.0 and 4.0, the failures being investigated in this paper are the victims of poor thermal design. But interestingly, the failures occurred when the operation was within the SOA. Which led to the recent analysis of a failure mode that manifests itself with a Base to Collector short.

Research has shown that when current filamentation, in a BJT power transistor, leads to a Base-Collector short, even within the specified SOA, it indicates a failure mode known as secondary breakdown[3].

Current Filamentation is a phenomenon that refers to the non-uniform distribution of current flow within the transistor's Base-Collector region. Instead of spreading evenly, the current concentrates into narrow, high-current paths or "filaments". These filaments can arise from instabilities within the device's structure or operating conditions.

This is a destructive failure mechanism unique to BJTs where current concentration occurs under high voltage and current conditions forming localized hotspots, due to the concentrated current.

The impedance of these hotspots decreases with increasing temperature, leading to further current concentration and causing uncontrolled positive feedback, also known as thermal runaway. This causes the device to rapidly overheat and degrade, ultimately leading to destruction. The failure mode is due to intense localized heating and melting within these current filaments causing a Base-Collector junction to short. This failure mode occurs even though the transistor is operating within the specified SOA.

The cited reference suggests proper thermal design will eliminate failures due to filamentation in pass transistors, as used in this analysis. High voltage switching and motor control designs have several other considerations, not of significance here.

The failures being analyzed, at least in the PS-15D-20A, occurred while bench testing with a 15 ADC load and 120VAC line. Even if the heat sink temperature was at 25^{o}C, the junction temperature would quickly rise to over 220^{o}C.

The PS-15D-( ) designs do not suffer from this failure mode due to proper thermal designs, for example the PS-15D-4 uses 3 pass transistors, as opposed to 2, much lower rectified DC voltage and proper heat sink size. Smaller heat sinks are suitable with forced air cooling.

6.0 PS-15D-4 Thermal Design

The thermal design starts with the electrical design. For example, the Astron RS-20M has a secondary voltage of 18.35 VAC with a 120.0 VAC line input. This results in excessive rectified DC voltage into the pass transistors, as mentioned previously.

Using the Astron transformer with a 12.6 VAC buck transformer, the secondary voltage is only 16.42 VAC with 120 VAC line voltage. At 110 VAC line, the secondary voltage is 14.89 VAC. This configuration provides adequate low line regulation while avoiding the Astron's entirely too high 18.38 VAC that produces the 20.85 VDC shown in Section 2.0.

A topic not covered in this paper is the filter capacitor selection. Many "rule of thumb" methods float about, but without exception, will not select the optimum capacitor. Suffice it to say, in this design the filter capacitor is 220,000 µF with a 19 A, 85^{o}C, ripple current rating.

However, the filter capacitor selection is a factor in the thermal design. Some "rule of thumb" selection methods base the capacitor value on ripple voltage, when actually

3. Toshiba Electronic Devices Corporation.

the selection is primarily based on the ripple current handling capability.

A capacitor with sufficient ripple current, for the a given load current, will inherently provide sufficient ripple voltage reduction. This design is an example, the 220,000 µF is selected to handle the 24.69 A_{RMS} ripple current, at 40°C design temperature. The resultant ripple voltage at 20 ADC load is 0.61 Vpp.

This brings us back to the thermal design. The minimum voltage across the pass transistors is desired, but with sufficient voltage margin at low line to ensure the ripple valley remains above the minimum voltage required for regulation. The PS-15D-( ) only needs an input DC voltage approximately 1.5V above the output voltage, or 15.30 V for a 13.80 VDC output voltage.

As already calculated with a 12.6 VAC buck transformer, at low line (110 VAC), the AC secondary voltage is 14.89 VAC and the ripple valley is 15.44 V.

With 120 VAC input the rectified DC, is 17.38 VDC (actually RMS with DC component). This is the value to be used to calculate pass transistor dissipation. So, all that is said to bring us back to the pass transistor thermal design.

Refer again to Figure 2.1 for the Pass Transistor configuration, except $R_E = 0.02\Omega$.

$$V_{RECT} = 17.38 \text{ VDC},$$
$$I_O = 20 \text{ ADC}.$$

$$V_{CE} = 17.3 - 13.85 - (6.67A \times 0.02\Omega), \text{ or}$$

$$V_{CE} = 3.40V.$$

Assuming the three transistors divide the load current equally (reasonable) then;

$$PD = V_{CE} \times I_C, \text{ and}$$

$$PD = 3.40V \times 6.67A$$

$$PD = 22.6W,$$

and of course the heat sink dissipation is;

67.80W.

The transistor junction temperature is given by;

$$T_J = 22.6W \times (1.17^oC/W + 0.17^oC/W) + T_S, \text{ and}$$

$$T_J = 30.36\,^oC + T_S.$$

The heat sink temperature and junction temperature are:

$$T_S = 67.80W \times 1.13^oC/W + 40^oC, \text{ or}$$

$$T_S = 116.61^oC, \text{ and}$$

$$T_J = 30.36\,^oC + 116.61^oC, \text{ or}$$

$$T_J = 146.97\,^oC.$$

These values are based on a lowered rectified DC voltage, that remains only a few volts above drop-out for the BJT in the common emitter configuration and the same size heat sink used in the previous analysis.

Also of note, the PS-15D-( ) series is designed for 100% duty cycle at the rated output current. At 20A output, 120 VAC input, 40°C ambient and 100% duty cycle the pass transistors are operating at 73.5% of rated SOA in stark contrast with the RS-20M operating at 121% of SOA - well actually only for a few minutes before failure and then only at 15 ADC load.

For additional safety, the heat sink effectiveness can be increased with forced air or larger surface. I have had successful design with 75% SOA operation.

The conclusion must be;

1. limiting of the rectified DC voltage to the minimum level required for regulation,

2. sufficient heat sink and

3. the use of proper number of pass transistors

are key to preventing the failure mode analyzed here.

In other words, a proper thermal design will keep a design out of the Base-Collector short failure mode.

Series Pass Transistor Design Considerations

7.0 RS-20M Refurbish to PS-15D-20B

Taking one last look at the old Astron power supply, I wondered if a way may yet exist to salvage it; pretty much as built. I realized the filter capacitor can be replaced with 3 ea. 22,000 µF CDE capacitors that are much smaller, but still provide 24 A_{RMS} ripple current capability. By replacing the overly large filter capacitor makes room for a buck transformer.

The buck transformer allows the rectified voltage to be reduced. Removing the rectifier from the heat sink removes 23.6W thermal load, allowing all of the heat sink capability to be used for cooling the pass transistors. The rectifier will be heat sinked to the chassis, as has been done in other versions of Astron power supplies.

The trade off of this approach is less margin for low line voltage. Some Astron power supplies regulate with as little as 102 VAC line voltage. In remote areas this may be a desirable feature, but in my shop the line voltage is seldom less than 115 VAC; during the summer, even with the A/C running.

Presented next is the buck transformer operation and thermal design with the above identified modifications.

Figure 7.1 shows the buck transformer inserted in series with the power transformer primary. Note the buck transformer primary and secondary phase, indicated by the polarity dots, provides a net voltage to the power transformer that is reduce by the buck transformer's secondary voltage.

The power transformer secondary voltage is calculated by the following equation;

$$V_{SEC} = [V_L - V_L(N_{SB}/N_{PB})] \div (N_P/N_S),$$

substituting known values and rearranging simplifies to

$$V_{SEC} = 0.135V_L.$$

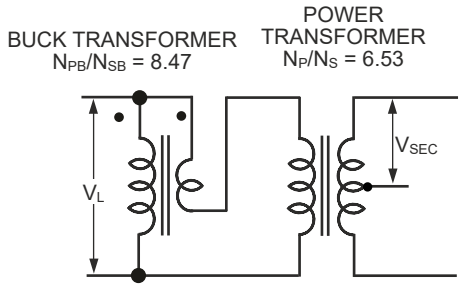


Figure 7.1. Buck transformer connections and turns ratio.

Table 7.1. Internal Voltages calculated vs line voltage.

V_L (V_{rms})	V_{SEC} (V_{rms})	V_{RECT} (V_{rms})[1]	V_{RV} (V_{DC})[1]	V_{CE} (V_{rms})[2,3]	$V_{CE(MIN)}$ (V_{PK})[3]
120.0	16.20	18.03	17.53	3.53	3.03
115.0	15.52	17.10	16.60	2.25	1.50
110.0	14.86	16.22	15.71	1.70	1.21

Table 7.1 shows the power supply internal voltages vs 110 to 120 VAC line voltage. These calculations are based on "Rectifier Design and Analysis" found on https://bwcelectronics.com. The load, used for these calculations, is 20 ADC with a 13.80 VDC output voltage.

For the PS-15D-( ) to maintain regulation, VCE needs to be at least 1.5V greater than the output voltage. So, this configuration will be marginal at 115 VAC and will loose regulation at 110 VAC with a 20 ADC load. However, with a 15 ADC load, the minimum VCE is 1.74V allowing operation with a low line of 110 VAC.

For low line voltage applications above 110 VAC, the 12.6 VAC buck transformer provides a more reasonable rectified and filtered DC voltage to the pass transistors. Perhaps even enough so that the Astron RS-20M can be salvaged with the two pass transistor configuration.

1. Ripple valley, the lowest voltage applied to the pass transistors.

2. Rectified and filtered voltage has major DC component, but also a ripple component. This is the RMS value of both, as needed to calculate heating.

3. Includes reduction due to voltage drops across R_E and R_{ISENSE}, a total of 0.5V.

Series Pass Transistor Design Considerations

Table 7.2. Internal Voltages **measured** vs line voltage.

V_L (V_{rms})	V_{SEC} (V_{rms})	V_{RECT} (V_{rms})[1]	V_{RV} (V_{DC})[1]	V_{CE} (V_{rms})[2,3]	$V_{CE(MIN)}$ (V_{PK})[3]
120.0	15.67	17.70	16.80	3.40	2.50
115.0	15.03	16.75	16.00	2.45	1.70
110.0	14.44	15.96	15.20	1.66	0.90

Pass transistor power and temperature calculations follow the same process used in Section 3.0. Except the 23.6W rectifier thermal load is removed from the pass transistor heat sink.

Figure 7.1 shows the PS-15D-20B pass transistors with current sense resistor R_{ISENSE} = 0.015Ω and R_E = 0.02Ω. Calculating for maximum pass transistor stress, the load is set to 20.0 ADC and line voltage to 120.0 VAC. Also, because measured values are available, they will be used in the calculations. As seen from Tables 7.1 and 7.2, the measured and calculated values are within 2 to 4% of one another.

$$V_{RECT} = 17.70 \text{ VDC},$$
$$I_O = 20 \text{ ADC}.$$

Thus;

$$V_{CE} = V_{RECT} - V_O - V_E, - V_{RISENSE} \text{ and}$$

$$V_{CE} = 3.40 \text{ VDC}.$$

It is reasonable to assume the two transistors divide the load current equally, therefore;

$$PD = V_{CE} \times I_C, \text{ and}$$

$$PD = 3.40V \times 10A$$

$$PD = 34.0W,$$

and of course the heat sink dissipation is;

68.0W.

The junction temperature is given by;

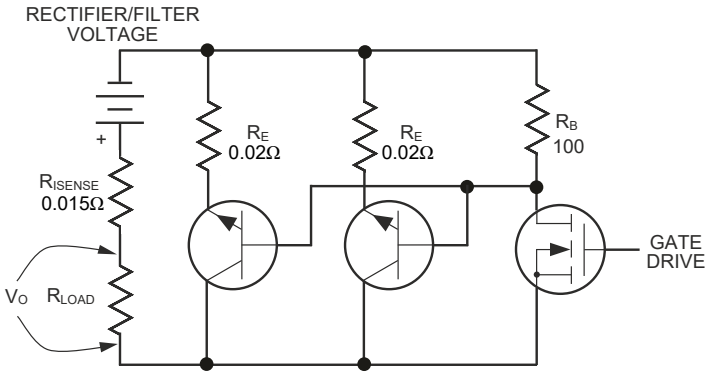


Figure 7.1. PS-15D-20B simplified pass transistor schematic.

$$T_J = P_D \times (\Theta_{JC} + \Theta_{CS}) + T_S \text{ and,}$$

$$T_J = 34.0W \times (1.17^oC/W + 0.17^oC/W) + T_S, \text{ and}$$

$$T_J = 45.56^oC + T_S.$$

Heat sink temperature is;

$$T_S = P_D \times \Theta_{SA} + T_A \text{ and,}$$

$$T_S = 68.0W \times 1.13^oC/W + 40^oC, \text{ or}$$

$$T_S = 116.84^oC, \text{ and}$$

$$T_J = 45.56^oC + 116.84^oC, \text{ or}$$

$$T_J = 162.36^oC.$$

The pass transistors junction temperature is now at 81.1% of SOA vs 121% with the Astron design. The Astron uses one of the emitter resistors to sense for current limit and Amp meter, where as the PS-15D-20B uses a stable wire wound resistor (the 0.015Ω).

The above calculations show that at 20A load and 120 VAC line the power supply should function. Now let us see what the thermal stress is with a 15.0 ADC Load.

At 120 VAC line voltage, 13.80 VDC output with a 15 ADC load the voltages are shown in Table 7.3. Calculating the thermal values;

$$PD = 4.34V \times 7.5A$$

$$PD = 32.55W,$$

Table 7.3. Internal Voltages with 15 ADC Load and 120 VAC Line.

V_L (V_{rms})	V_{SEC} (V_{rms})	V_{RECT} (V_{rms})[1]	V_{RV} (V_{DC})[1]	V_{CE} (V_{rms})[2,3]	$V_{CE(MIN)}$ (V_{PK})[3]
120.0	15.67	18.64	17.90	4.34	3.60

and of course the heat sink dissipation is;

65.10W.

The junction temperature is given by;

$$T_J = P_D \times (\Theta_{JC} + \Theta_{CS}) + T_S \text{ and,}$$

$$T_J = 32.5W \times (1.17^oC/W + 0.17^oC/W) + T_S, \text{ and}$$

$$T_J = 43.62\,^oC + T_S.$$

Heat sink temperature is;

$$T_S = P_D \times \Theta_{SA} + T_A \text{ and,}$$

$$T_S = 65.10W \times 1.13^oC/W + 40^oC, \text{ or}$$

$$T_S = 113.56^oC, \text{ and}$$

$$T_J = 43.62\,^oC + 113.56^oC, \text{ or}$$

$$T_J = 157.18\,^oC.$$

The pass transistors are now operating at 78.6% of SOA. Even though my design goal is 60 to 65%, this thermal load should allow the power supply to operate fine in most applications.

Even though Astron rates the RS-20M for 16 ADC continuous (a condition where the pass transistors failed after a few minutes), we will see on the next page, using measured data, 15 ADC continuous Load is now acceptable with the buck transformer design. 20A load operation should be limited to 35% duty cycle with a maximum dwell time of 3 minute.

7.0 Results of RS-20M Refurbish to PS-15D-20B

Figure 8.1 is shows the finished product after refurbish; operating with a continuous 15 ADC Load and 120 VAC Line. Load regulation from 0 to 15 ADC is 0.16%, at the power supply terminals. Current limit is 24 ADC with load dependent fold back.

Figure 8.1 Finished refurbished power supply with 15 ADC Load.

Using measured V_{CE} the thermal performance can be compared to the calculated performance.

Measured V_{CE} = 3.64 VDC and thermal calculations are;

$$PD = 3.64V \times 7.5A$$

$$PD = 27.30W,$$

and of course the heat sink dissipation is;

54.6W.

The junction temperature is given by;

$$T_J = P_D \times (\Theta_{JC} + \Theta_{CS}) + T_S \text{ and,}$$

$$T_J = 27.30W \times (1.17^oC/W + 0.17^oC/W) + T_S, \text{ and}$$

$$T_J = 36.58\,^oC + T_S.$$

Heat sink temperature is;

$$T_S = P_D \times \Theta_{SA} + T_A \text{ and,}$$

$$T_S = 54.6W \times 1.13^oC/W + 25^oC, \text{ or}$$

T_S = 86.69°C, and

T_J = 36.58 °C + 86.69°C, or

T_J = 123.28 °C,
or 61.6% of SOA.

The previous calculations were done for a stand alone heat sink with the surface area of the Astron heat sink. However, the heat sink θ_{SA} of 1.13°C/W measures 0.74°C/W when the power supply is tested on the bench with 15 ADC Load and 120.0 VAC Line which calculates the actual Θ_{SA} as;

ΔT_{SA} = 65.30°C - 25°C, or

ΔT_{SA} = 40.3°C, and

Θ_{SA} = 40.3°C ÷ 54.6W, and

Θ_{SA} = 0.74°C/W.

Notice the measured values are at T_A = 25°C.

Measured thermal performance is 35% better than the calculations determined, for the heat sink alone. The primary contribution to improved thermal performance is due to the heat sink being mounted onto the chassis; which adds considerably more surface area, even if the effect diminishes as heat travels around the surface, away from the heat source.

The good news is the refurbished power supply has more margin than previously calculated. In this case, that is a positive, but if designing from scratch, it is prudent to consider the chassis' contribution.

Figure 8.2 shows the internal wiring of the PS-15D-20B. The PS15D120 Regulator Assembly is attached to the output terminals with copper angle brackets. The 66,000 µF filter capacitor bank is on the left, behind the voltmeter. The filter capacitors are PCB TH soldered into a custom PCB.

The buck transformer is in the foreground with the power transformer in the background and the rectifier to the right of the buck transformer. The pass transistors are mounted on the heat sink, but not visible here.

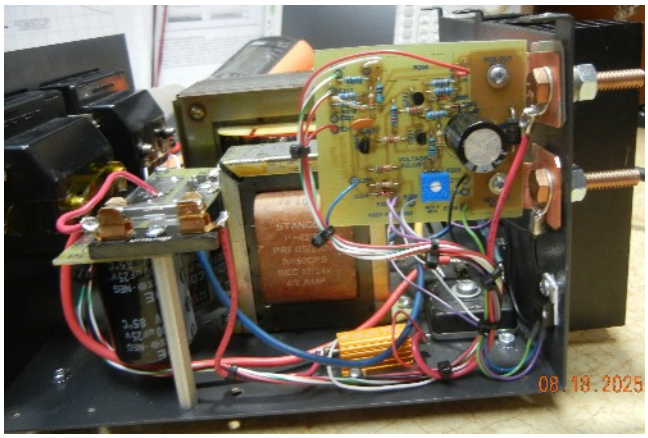


Figure 8.2 PS-15D-20B internal wiring.

Several temperature test were performed at 15ADC Load and 120 VAC Line for 20 minutes each. The heat sink stabilized at approximately 15 minutes during each run. The bench temperature was 25°C with only slight room air movement from the HVAC.

Testing was also conducted at 20 ADC and 120 VAC for 2 and 4 minutes with continuous Load. The buck transformer and fuse were uncomfortable to touch, actual temperature not measured, but no areas of concern were identified.

Fold-back current limiting was measured at 24.1 ADC and limited before the 20A DC fuse opened. When the initial failure occurred, D203 shorted and had to be replaced.

9.0 Conclusion

In this paper, the Astron pass transistor Base to Collector failure was identified. Proper thermal design was shown to theoretically correct the B-C failures and then was confirmed with an actual refurbish of the failed power supply. During the process the PS-15D-4 was also shown to be adequate and immune from the current filamentation failure mode introduced in this analysis.